

February 10, 2004

To: Commissioner for Patents P.O. Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/736,943 12/16/03

Wenhe Lin et al.

METHODS TO FORM DUAL METAL GATES BY INCORPORATING METALS AND THEIR CONDUCTIVE OXIDES

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Steph Backer 2/12/04

CS-00-114BD

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- U.S. Patent 6,043,157 to Gardner et al., "Semiconductor Device Having Dual Gate Electrode Material and Process of Fabrication Thereof," discloses a process for forming dual gates where one gate is polysilicon and the other gate is metal.
- U.S. Patent 6,087,231 to Xiang et al., "Fabrication of Dual Gates of Field Transistors with Prevention of Reaction Between the Gate Electrode and the Gate Dielectric with a High Dielectric Constant," discloses a dummy gate process where amorphous gates doped with different dopants are formed.
- U.S. Patent 6,083,836 to Rodder, "Transistors with Substitutionally Formed Gate Structures and Method," teaches a dummy gate process where two gates are formed.
- U.S. Patent 5,266,519 to Iwamoto, "Method for Forming a Metal Conductor in Semiconductor Device," teaches oxidation of a metal film to be used as an anti-plating mask.
- U.S. Patent Application CS-00-115, Serial #09/981,415, filed on 10/18/01, assigned to the same assignee, now issued as U.S. 6,475,908, describes methods for forming dual-metal gate CMOS transistors.

Sincerely,

Stephen B. Ackerman, Reg. #37761

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